AMENDMENTS TO THE CLAIMS

The following is a complete list of all claims in this application.

24. (Previously Presented) A liquid crystal display (LCD), comprising:

a liquid crystal panel having a plurality of pixels;

a timing control circuit generating a gate clock signal and a plurality of control signals;

a gray voltage generation circuit generating a first gray voltage in a first interval of the gate clock signal and a second gray voltage in a second interval of the gate clock signal in response to a voltage level of the gate clock signal and a plurality of reference voltages obtained by dividing a power supply voltage to a predetermined ratio, the first gray voltage having a magnitude greater than that of the second gray voltage;

a gate driving circuit sequentially scanning the pixels row by row in response to the gate clock signal; and

a source driving circuit generating a first driving voltage corresponding to the first gray voltage and a second driving voltage corresponding to the second gray voltage,

wherein the first driving voltage is applied to the panel in the first interval of the gate clock signal and the second driving voltage is applied to the panel in the second interval of the gate clock signal.

25. (Previously Presented) The LCD of claim 24, wherein the source driving circuit, while driving a positive polarity of the panel, generates a driving voltage having a

first voltage level in the first interval of the gate clock signal, and generates a driving voltage having a second voltage level in the second interval of the gate clock signal, and

both the first voltage level and the second voltage level are higher than a common voltage level, and the first driving voltage level is higher than of the second driving voltage level.

26. (Previously Presented) The LCD of claim 25, wherein the source driving circuit, while driving a negative polarity of the panel, generates a driving voltage having a third voltage level in the first interval of the gate clock signal, and generates a driving voltage having a fourth voltage level in the second interval of the gate clock signal, and

both the first voltage level and the second voltage level are lower than the common voltage level, and the third driving voltage level is lower than the fourth driving voltage level.

27. (Previously Presented) The LCD of claim 24, wherein the gray voltage generation circuit comprises:

a clock generator generating a plurality of clock signals having a same period as the gate clock signal, in response to the gate clock signal;

a voltage generator dividing the power supply voltage to a predetermined ratio to generate a plurality of voltages as reference for generating the first gray voltage and the second gray voltage; and

a gray voltage generator outputting either the first gray voltage or the second gray voltage to the source driving circuit, in response to the gate clock signals issued from the clock generator and the voltages generated by the voltage generator.

28. (Previously Presented) The LCD of claim 27, wherein the clock generator comprises:

an input terminal for receiving the gate clock signal;

n-bit clock generation units coupled to the input terminal in parallel; and

n-bit output terminals each being coupled to the n-bit clock generation units,

wherein each of the clock generation units has a capacitor and a resister that are serially connected between the input terminal and the output terminal, and generates a clock signal having a same period as the gate clock signal.

29. (Previously Presented) The LCD of claim 27, wherein the voltage generator includes n-bit voltage generation units for dividing the power supply voltage to a predetermined ratio to generate the n-bit voltages each having different voltage level, and

wherein each of the voltage generation unit includes at least two and more resisters coupled between the power supply voltage and a ground voltage, and an output terminal coupled to one of contact points between the resisters.

30. (Previously Presented) The LCD of claim 27, wherein the gray voltage generator comprises:

a positive gray voltage generation unit for generating (m/2)-bit positive first and second gray voltages having a same polarity as the gate clock signal and each having different voltage level in the first interval and the second interval of the gate clock signal so as to drive a positive polarity of the panel; and

a negative gray voltage generation unit for generating (m/2)-bit negative first and second gray voltages having a polarity opposite to the gate clock signal and each having different voltage level in the first interval and the second interval of the gate clock signal so as to drive a negative polarity of the panel.

31. (Previously Presented) The LCD of claim 30, wherein the positive gray voltage generation unit includes at least one or more amplifier circuits having a first input terminal for receiving one of the n-bit clock signals from the clock generator and one of the n-bit reference voltages from the voltage generator, a second input terminal connected to a ground through a resister, and an amplifier circuit having a feedback resister connected between the second input terminal and the output terminal.

32. (Previously Presented) The LCD of claim 31, wherein the amplifier circuit adds the clock signal to the reference voltage, and amplifies the same to generate the positive first and second gray voltages.

33. (Previously Presented) The LCD of claim 31, wherein the amplifier circuit further includes a resister for dividing the positive first and second gray voltages, and an

output terminal connected to the contact point of the resister, for outputting the divided gray voltage.

34. (Previously Presented) The LCD of claim 30, wherein the negative gray voltage generation unit includes a first input terminal for receiving one of the n-bit reference voltages from the voltage generator, a second input terminal for receiving one of the n-bit clock signals from the clock generator, and an amplifier circuit having a feedback resister connected between the second input terminal and the output terminal.

35. (Previously Presented) The LCD of claim 34, wherein the amplifier circuit subtracts the clock signal from the reference voltage, and amplifies it to a predetermined ratio to generate the negative first and second gray voltages.

36. (Previously Presented) The LCD of claim 34, wherein the amplifier circuit further includes a resister for dividing the negative first and second gray voltages, and an output terminal connected to the contact point of the resister, for outputting the divided gray voltage.